Microelectronics Roadmap

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Department of Defense
OFFICE OF PREPUBLICATION AND SECURITY REVIEW

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28 May 2024

SLIDES ONLY

NO SCRIPT PROVIDED

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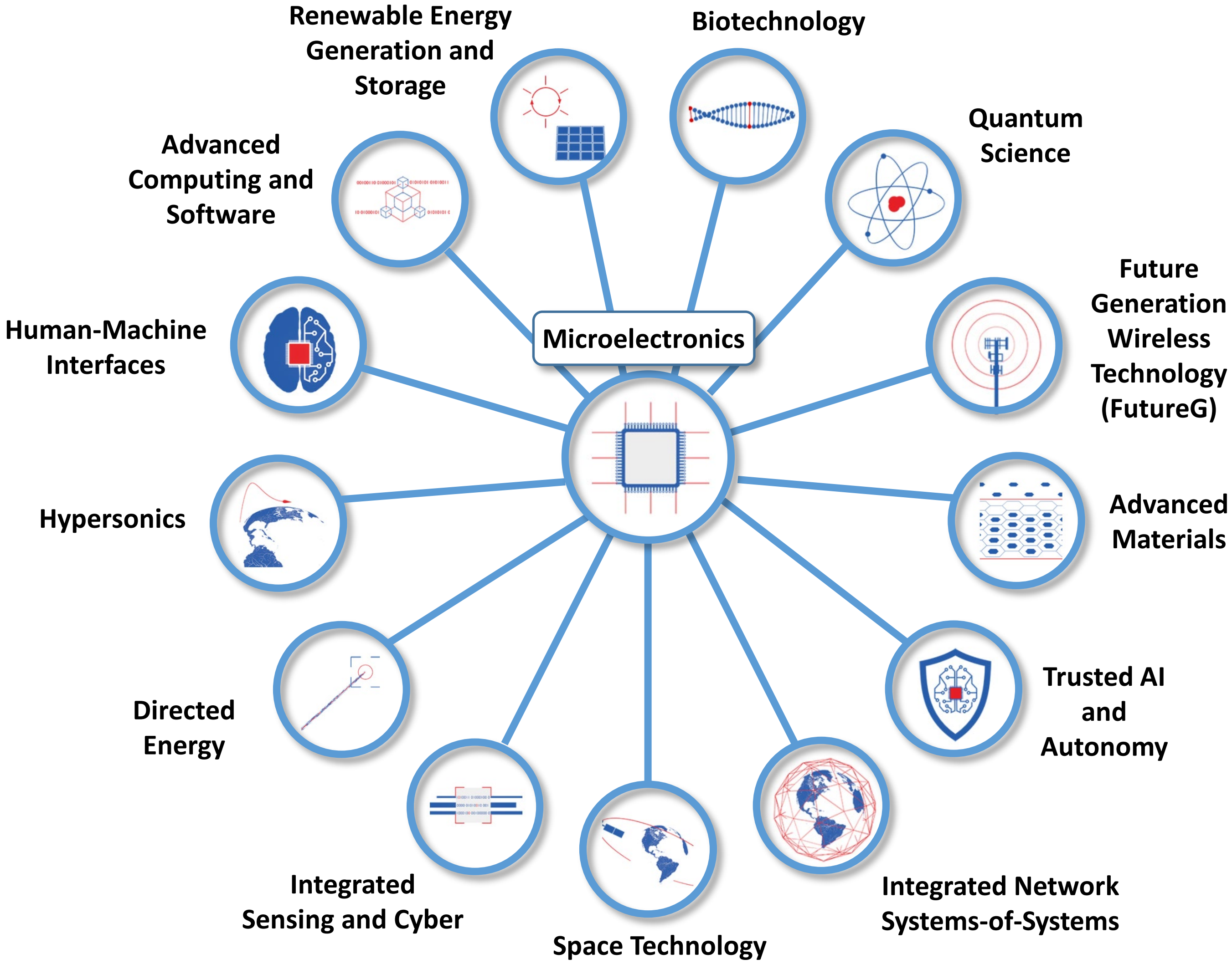
DEPARTMENT OF DEFENSE

Critical Technology Area Synergies: Microelectronics



Autonomous Drones

AI Chips

Self Driving Vehicles

Energy Efficiency For Edge Computing

Military Applications

DoD Microelectronics Vision

Microelectronics vision statement for the Department:

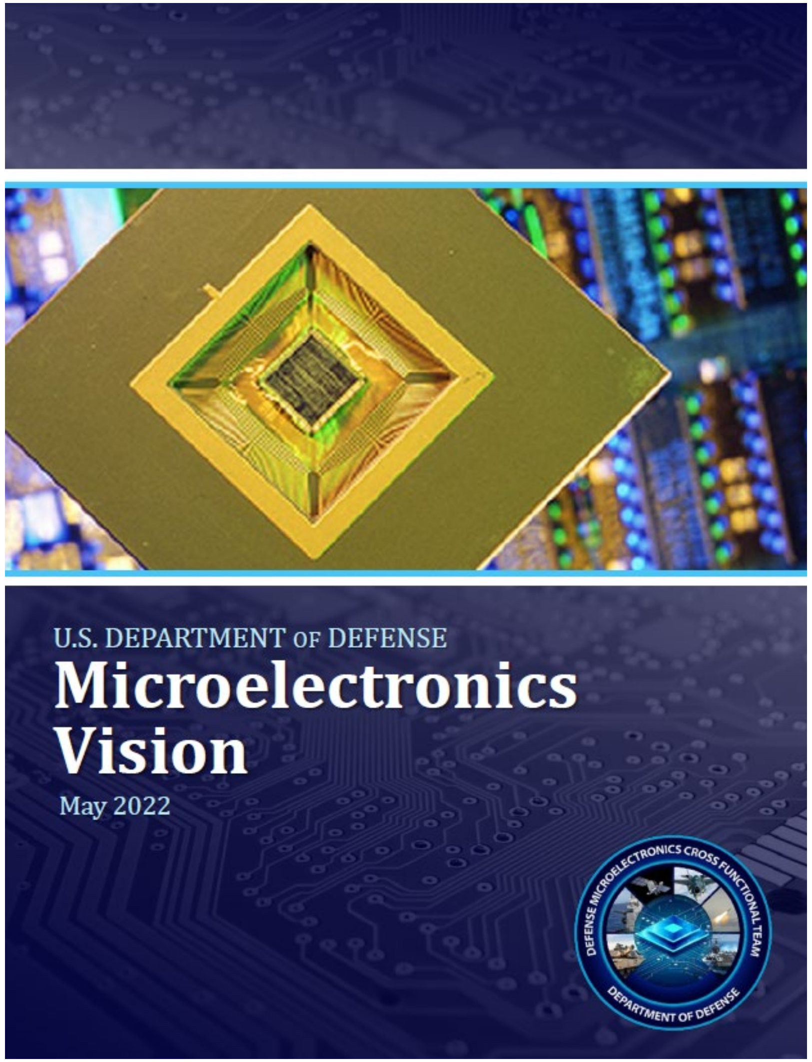
DoD will obtain and sustain guaranteed, long-term access to measurably secure microelectronics that enable overmatch, increased operational availability, and support Warfighter combat readiness.

"The Department will continue to invest in programs to secure U.S. microelectronics interests; reverse the erosion of domestic innovation and supply; and establish a strong foundation for the next generation of microelectronics technology for DoD applications, while also sustaining current systems."

Lloyd J. Austin III
Secretary of Defense

Heidi Shyu
Under Secretary of Defense for
Research and Engineering

William A. LaPlante
Under Secretary of Defense for
Acquisition and Sustainment

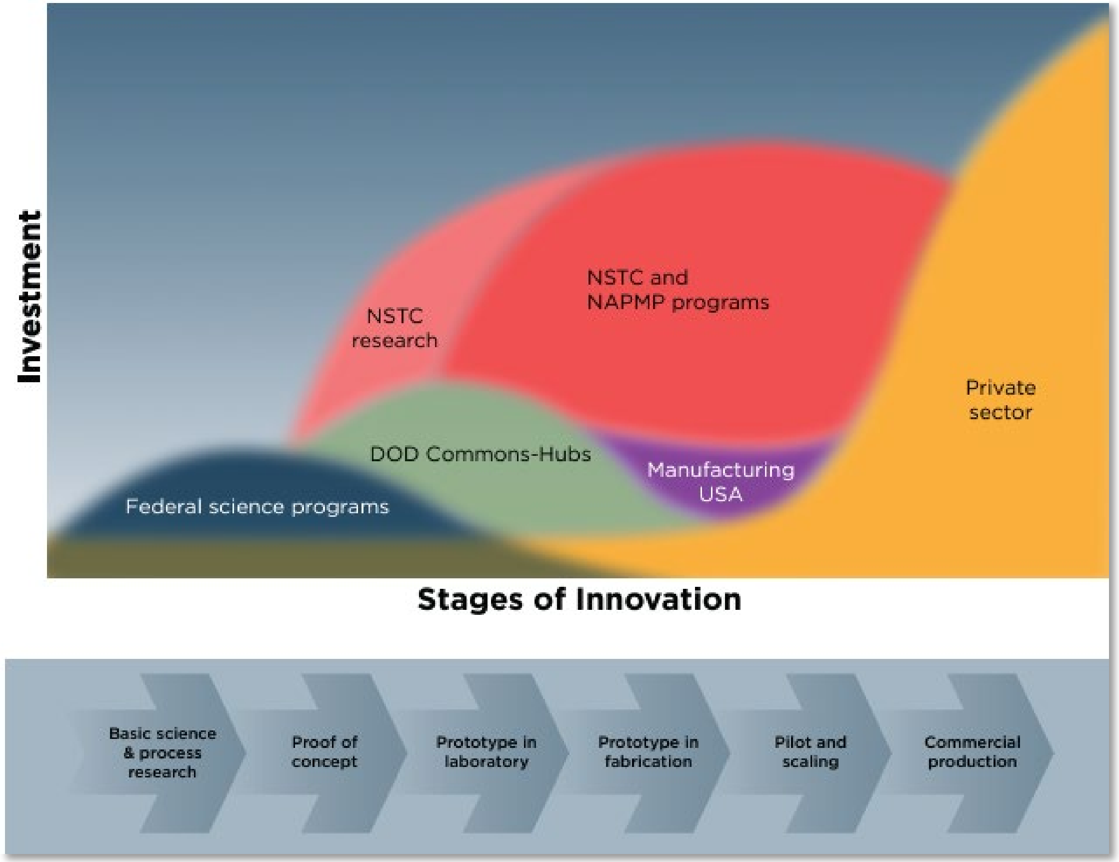


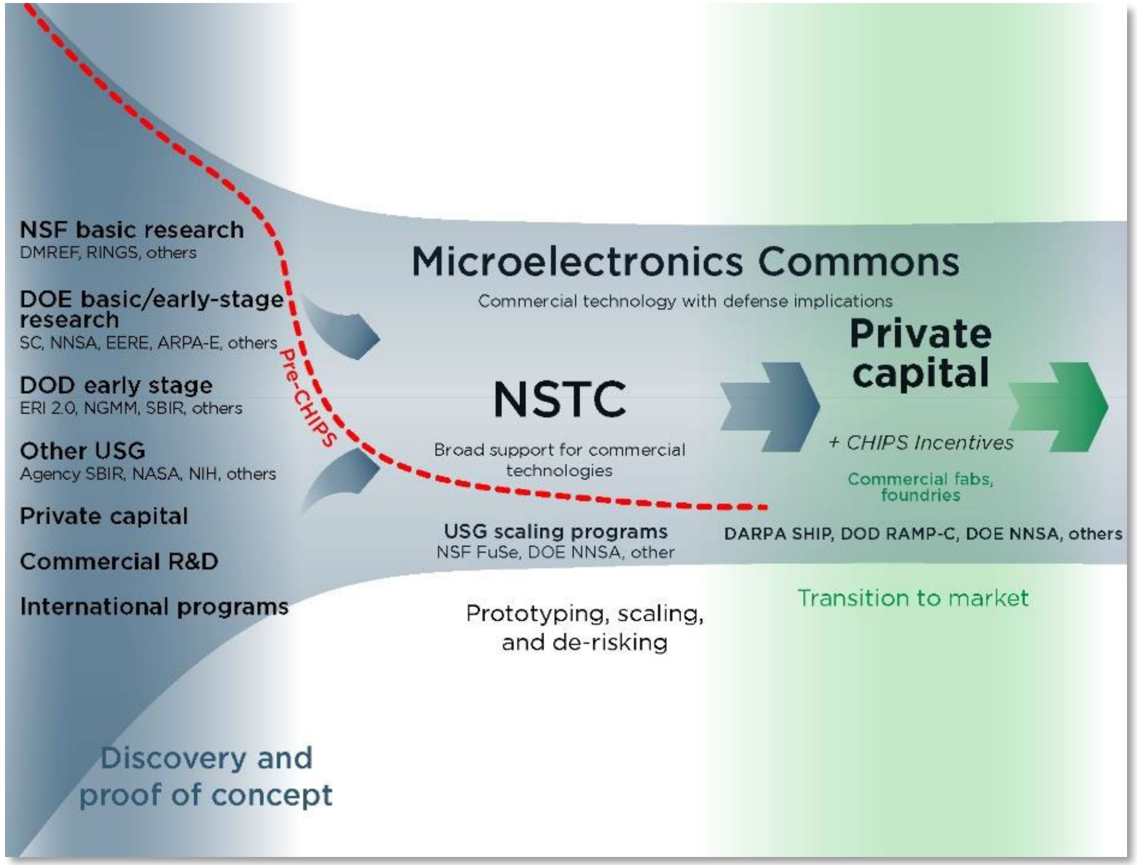
U.S. DEPARTMENT OF DEFENSE
Microelectronics
Vision
May 2022

Defense Microelectronics Cross Functional Team
Department of Defense

CHIPS and Science Act Offers a Whole of Government Approach

The National Semiconductor Technology Center (NSTC) and Microelectronics Commons will expand the number of concepts and ideas that can transition from proof-of-concept to the market.

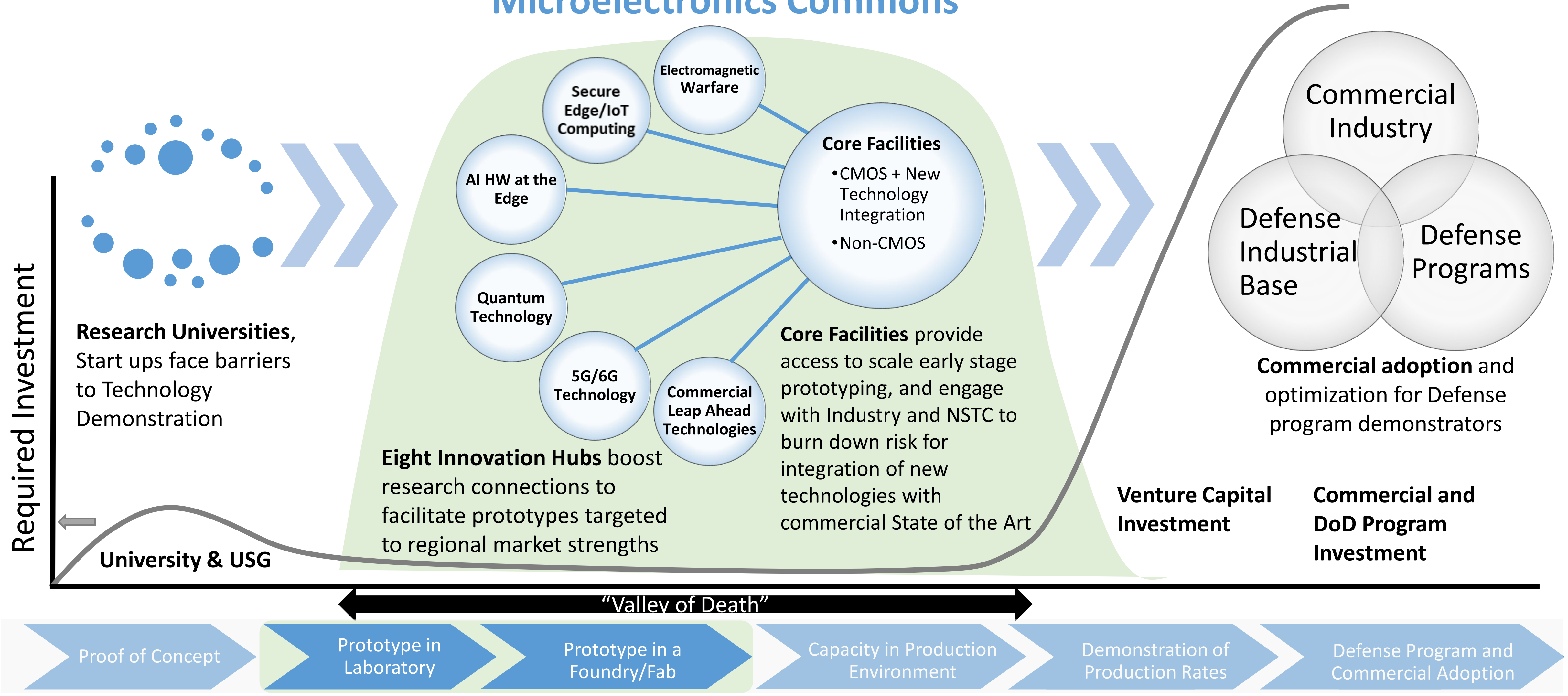




https://www.nist.gov/system/files/documents/2023/04/27/A%20Vision%20and%20Strategy%20for%20the%20NSTC.pdf

Microelectronics Commons Addresses the Valley of Death

Microelectronics Commons



Required Investment

Research Universities, Start ups face barriers to Technology Demonstration

University & USG

Secure Edge/IoT Computing

Electromagnetic Warfare

AI HW at the Edge

Quantum Technology

5G/6G Technology

Commercial Leap Ahead Technologies

Core Facilities

- CMOS + New Technology Integration
- Non-CMOS

Eight Innovation Hubs boost research connections to facilitate prototypes targeted to regional market strengths

Core Facilities provide access to scale early stage prototyping, and engage with Industry and NSTC to burn down risk for integration of new technologies with commercial State of the Art

Commercial Industry

Defense Industrial Base

Defense Programs

Commercial adoption and optimization for Defense program demonstrators

Venture Capital Investment

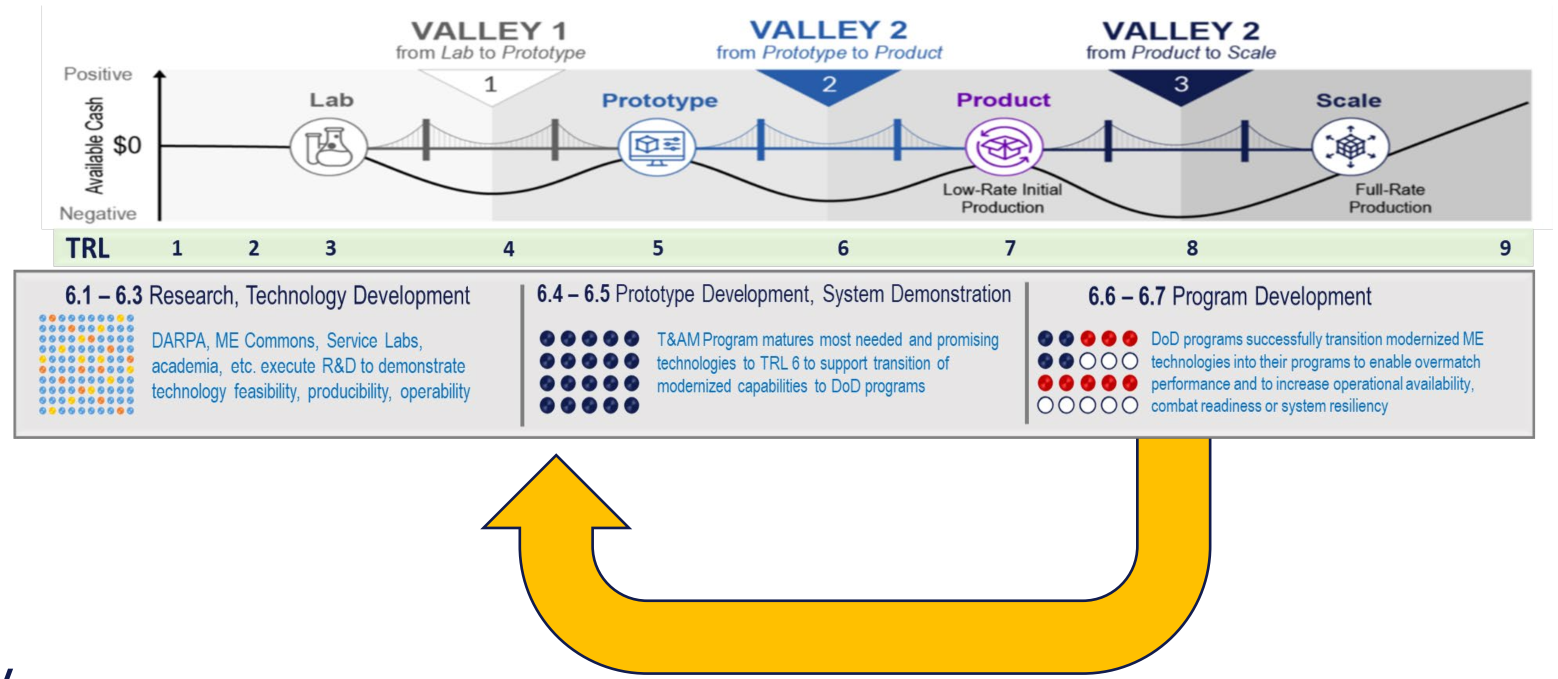
Commercial and DoD Program Investment

"Valley of Death"

Proof of Concept → Prototype in Laboratory → Prototype in a Foundry/Fab → Capacity in Production Environment → Demonstration of Production Rates → Defense Program and Commercial Adoption

Trusted and Assured Microelectronics Program Vision

- Drive access to advanced microelectronics technologies that leverage commercial capabilities, tools, techniques and practices to meet Department operational needs
- Accelerate transition of capabilities to the Military Services and Combatant Commands in support of the 2022 National Defense Strategy and the 2023 National Defense Science and Technology Strategy
- Identify and work to mitigate persistent threats throughout the microelectronics supply chain



6.1 – 6.3 Research, Technology Development

DARPA, ME Commons, Service Labs, academia, etc. execute R&D to demonstrate technology feasibility, producibility, operability

6.4 – 6.5 Prototype Development, System Demonstration

T&AM Program matures most needed and promising technologies to TRL 6 to support transition of modernized capabilities to DoD programs

6.6 – 6.7 Program Development

DoD programs successfully transition modernized ME technologies into their programs to enable overmatch performance and to increase operational availability, combat readiness or system resiliency

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Progression from Concept to Product

Microelectronics Commons

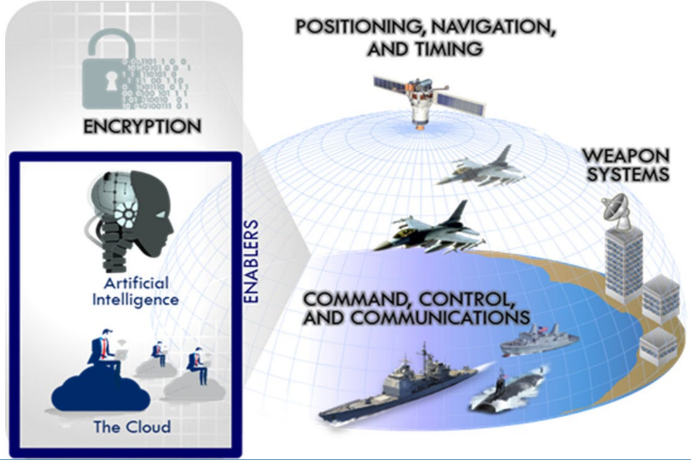
- Electronic Warfare
- Secure Edge/IoT Computing
- AI HW at the Edge
- Quantum Technology
- 5G/6G Technology
- Commercial Leap Ahead Technologies

Tech Demos

- RAMP
- RAMP-C
- SHIP
- T&AM Prototypes

Application Platforms

- Aircraft
- Submarines
- Ships
- Space Systems
- Ground Systems
- Missile Defense
- C4ISR



Artist Rendering
Background Image: Edwards Air Force Base

Lab-to-fab prototyping bridges valley of death from laboratory research to foundry/fab prototyping

Education and Workforce Development Roadmap

<u>FY23 Baseline **Students**</u>
- ✓ **675 Enrolled** ★
- ✓ 262 Graduated
- ✓ ~175 to Defense

<u>FY29 Plan Students</u>
- **~3,000 Enrolled** ☆
- ~2,000 Graduates
- ~1,400 to Defense

<u>Modeling assumptions</u>
- +10% YOY enroll > 2025
- ~ 25% annual grad rate
- ~ 2/3 to defense sector

MISSION: DoD NEED	Focus Areas	FY2024	FY2025	FY2026	FY2027	FY2028	FY2029	FY2030	FY2031	FY2032	FY2033	10 Year Vision
ATTRACT EXPOSURE	K-12 Teachers & Districts	K-12 pilot, promotion		K-12 expansion beyond pilot, other states (Minnesota, Ohio)								**Awareness** as desired profession: diverse education & career paths from factory technician to PhD level with role models across country
	Summer internships	Summer internships at public and private facilities										
	Veterans outreach	Initial study	Veterans outreach pilot, then expansion for untapped, clearable talent pool									
	Women's initiative	Women's pilot		Women's expansion beyond pilot for untapped talent pool								
	Universities, attract HBCU		Grow SCALE academic partners									
DEVELOP EDUCATION	K-12 teacher PD, guides	Update K-12, university, other curriculum based on technical area Knowledge, Skills, and Abilities needs assessments										**Knowledge superiority for US** across topics, access creating next generation leadership
	SCALE curriculum growth	nanoHub	SCALE & MEST content (courses, software, etc.) contribution growth via nanoHub									
	MEST continuous content		MEST organizations contributing content across Public Private Academia Partnerships									
MAINTAIN EXPERIENCE	SCALE, MEST	Twice annual SCALE Performative report										**Ready workforce** fuels US Defense sector & US Microelectronics industry providing global stability & growth
	DoD Facility / Lab access		Increase access at DoD facility and labs as recommended by DoD Workforce strategic plan									
	DoD ME WF roadmap	Update DoD Microelectronics Workforce needs / roadmap										

K-12 = 3 years
RH = 2 ½ years
Vets = 1 year study
Women = 2 years
Internship cost share

- Radiation Effects, Rad Hard
- Advanced Packaging, Heterogeneous Integration
- System on Chip (SOC)
- Embedded / Trusted AI
- Supply Chain Awareness
- Radio Frequency- & Opto-Electronics (RF/OE)

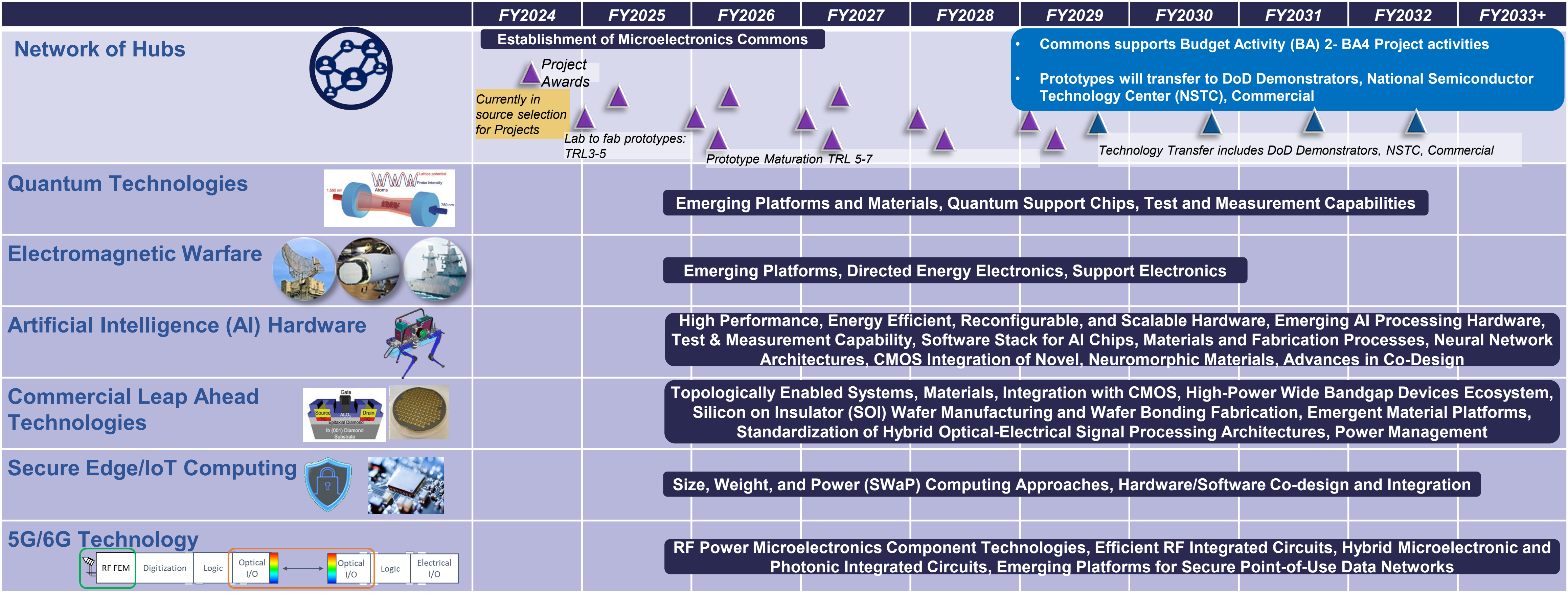
Enabling growth with reinforcing, cyclical interactions for Ready US WF:

- Attract, re-skill existing / adjacent engineers, technicians, users (veterans)
- Public Private Academia Partnership consortia
- Microelectronic topics into STEM mainstream, e.g. Mechanical Engineering +
- Public Private Facility / Lab Tours, collaborations, exchanges, internships

Data-driven investments based on stakeholder needs

K-12 STEM · Technical Certificates · Undergraduate · Master's · PhD · Existing Workforce · Microelectronics Leadership

Microelectronics Commons Roadmap



Network of Hubs

Establishment of Microelectronics Commons

Project Awards

Currently in source selection for Projects

Lab to fab prototypes: TRL3-5

Prototype Maturation TRL 5-7

- **Commons supports Budget Activity (BA) 2- BA4 Project activities**
- **Prototypes will transfer to DoD Demonstrators, National Semiconductor Technology Center (NSTC), Commercial**

Technology Transfer includes DoD Demonstrators, NSTC, Commercial

Quantum Technologies

Emerging Platforms and Materials, Quantum Support Chips, Test and Measurement Capabilities

Electromagnetic Warfare

Emerging Platforms, Directed Energy Electronics, Support Electronics

Artificial Intelligence (AI) Hardware

High Performance, Energy Efficient, Reconfigurable, and Scalable Hardware, Emerging AI Processing Hardware, Test & Measurement Capability, Software Stack for AI Chips, Materials and Fabrication Processes, Neural Network Architectures, CMOS Integration of Novel, Neuromorphic Materials, Advances in Co-Design

Commercial Leap Ahead Technologies

Topologically Enabled Systems, Materials, Integration with CMOS, High-Power Wide Bandgap Devices Ecosystem, Silicon on Insulator (SOI) Wafer Manufacturing and Wafer Bonding Fabrication, Emergent Material Platforms, Standardization of Hybrid Optical-Electrical Signal Processing Architectures, Power Management

Secure Edge/IoT Computing

Size, Weight, and Power (SWaP) Computing Approaches, Hardware/Software Co-design and Integration

5G/6G Technology

RF Power Microelectronics Component Technologies, Efficient RF Integrated Circuits, Hybrid Microelectronic and Photonic Integrated Circuits, Emerging Platforms for Secure Point-of-Use Data Networks

Creating a network of U.S regional innovation hubs to foster a pipeline of talent and accelerate lab-to-fab prototyping

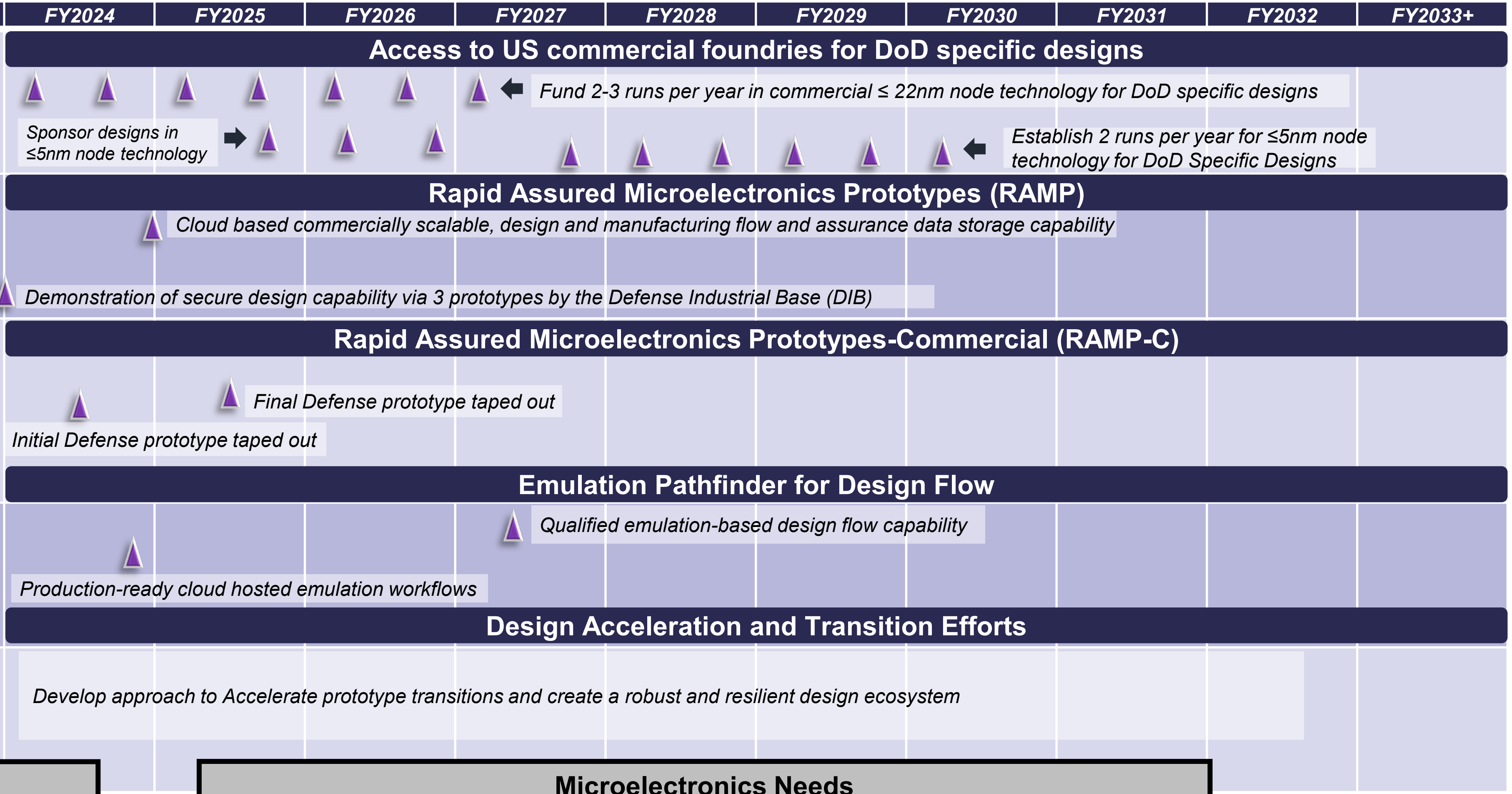
LEGEND

Enhanced Capabilities

▲ *Key Milestones* ▲ *Options*

- "Lab-to-Fab" testing/prototyping network for microelectronics technologies
- Broad access to prototyping capabilities through augmented regional facilities
- Education and training of students to produce a robust semiconductor talent pipeline

Access to State of the Art Microelectronics Roadmap



Foundry Access

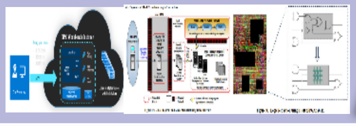
Access to US commercial foundries for DoD specific designs

▲ ▲ ▲ ▲ ▲ ▲ ▲ *Fund 2-3 runs per year in commercial ≤ 22nm node technology for DoD specific designs*

Sponsor designs in ≤5nm node technology ▲ ▲ ▲

▲ ▲ ▲ ▲ ▲ ▲ *Establish 2 runs per year for ≤5nm node technology for DoD Specific Designs*

Rapid Assured Microelectronics Prototypes (RAMP)



Rapid Assured Microelectronics Prototypes (RAMP)

▲ *Cloud based commercially scalable, design and manufacturing flow and assurance data storage capability*

▲ *Demonstration of secure design capability via 3 prototypes by the Defense Industrial Base (DIB)*

Rapid Assured Microelectronics Prototypes-Commercial (RAMP-C)

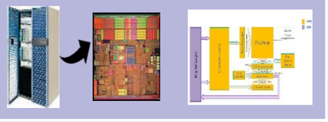
Rapid Assured Microelectronics Prototypes-Commercial (RAMP-C)

▲ *Final Defense prototype taped out*

▲ *Initial Defense prototype taped out*

Emulation Pathfinder for Design Flow

Cloud and Electronic Design Automation (EDA)



▲ *Qualified emulation-based design flow capability*

▲ *Production-ready cloud hosted emulation workflows*

Design Acceleration and Transition Efforts

Design Acceleration and Transition (D2TA)

Develop approach to Accelerate prototype transitions and create a robust and resilient design ecosystem

LEGEND

Enhanced Capabilities

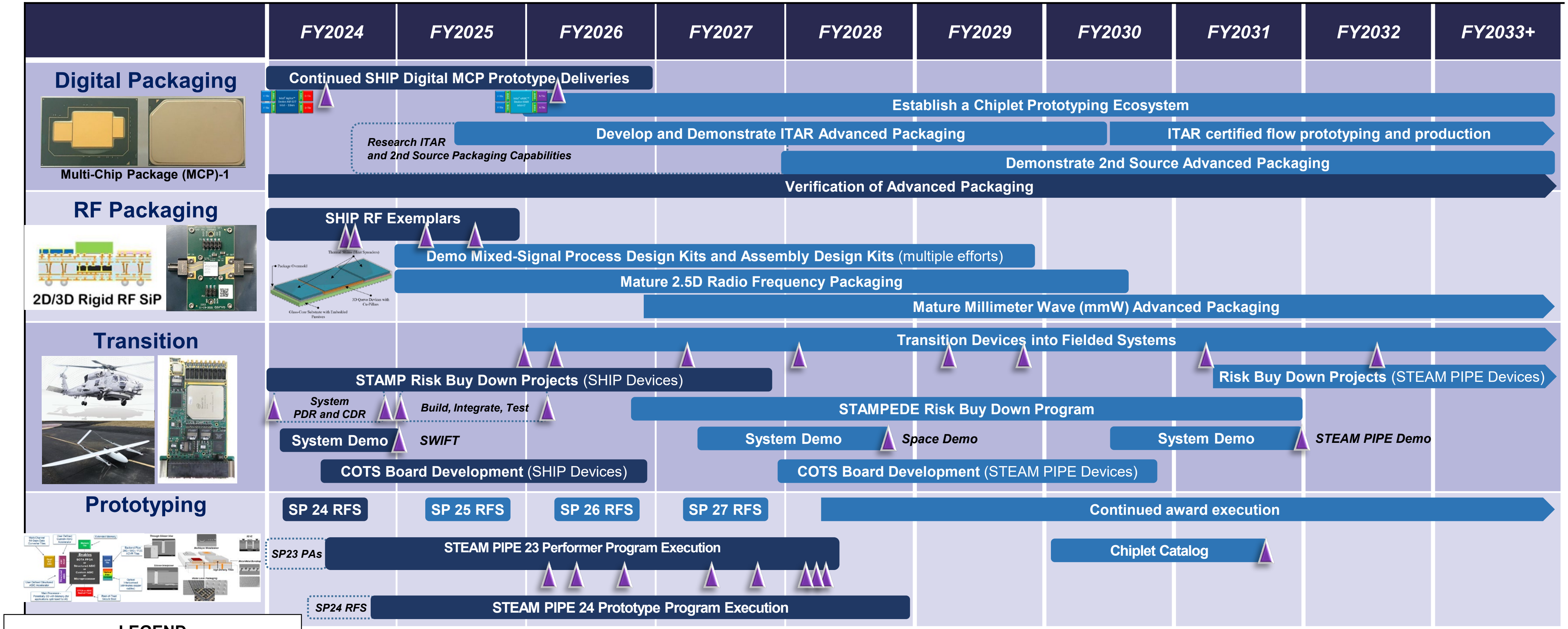
▲ *Key Milestones*

Microelectronics Needs

- Domestic access to mature materials, foundries, and packaging
- Ecosystem alignment to Defense program needs

Major Investments to Mature the Domestic Microelectronics Ecosystem

Access to Advanced Packaging and Test Roadmap



FY2024 | FY2025 | FY2026 | FY2027 | FY2028 | FY2029 | FY2030 | FY2031 | FY2032 | FY2033+

Digital Packaging

Multi-Chip Package (MCP)-1

Continued SHIP Digital MCP Prototype Deliveries

Establish a Chiplet Prototyping Ecosystem

Research ITAR and 2nd Source Packaging Capabilities

Develop and Demonstrate ITAR Advanced Packaging

ITAR certified flow prototyping and production

Demonstrate 2nd Source Advanced Packaging

Verification of Advanced Packaging

RF Packaging

2D/3D Rigid RF SiP

SHIP RF Exemplars

Demo Mixed-Signal Process Design Kits and Assembly Design Kits (multiple efforts)

Mature 2.5D Radio Frequency Packaging

Mature Millimeter Wave (mmW) Advanced Packaging

Transition

Transition Devices into Fielded Systems

STAMP Risk Buy Down Projects (SHIP Devices)

Risk Buy Down Projects (STEAM PIPE Devices)

System PDR and CDR

Build, Integrate, Test

STAMPEDE Risk Buy Down Program

System Demo *SWIFT*

System Demo *Space Demo*

System Demo *STEAM PIPE Demo*

COTS Board Development (SHIP Devices)

COTS Board Development (STEAM PIPE Devices)

Prototyping

SP 24 RFS

SP 25 RFS

SP 26 RFS

SP 27 RFS

Continued award execution

SP23 PAs

STEAM PIPE 23 Performer Program Execution

Chiplet Catalog

SP24 RFS

STEAM PIPE 24 Prototype Program Execution

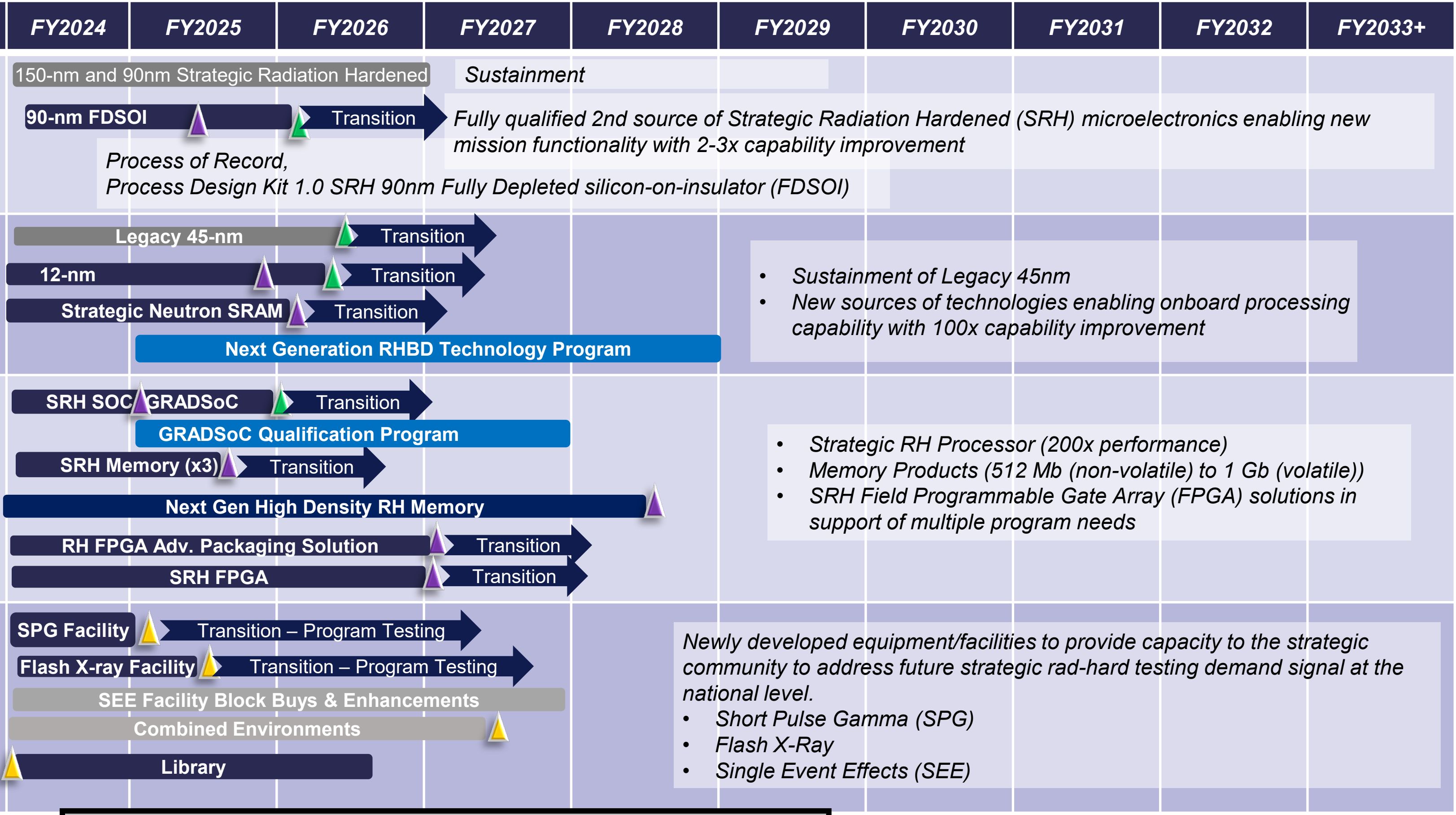
LEGEND

Key Milestone

Enhanced Capabilities

Follow-on Capabilities

Radiation Hardened Microelectronics Roadmap



Radiation Hardened by Process (RHBP)

150-nm and 90nm Strategic Radiation Hardened

Sustainment

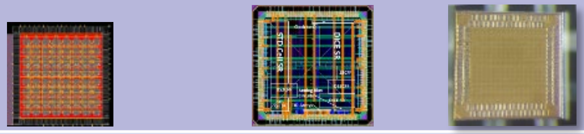
90-nm FDSOI

Transition

Fully qualified 2nd source of Strategic Radiation Hardened (SRH) microelectronics enabling new mission functionality with 2-3x capability improvement

Process of Record,
Process Design Kit 1.0 SRH 90nm Fully Depleted silicon-on-insulator (FDSOI)

Radiation Hardened by Design (RHBD)



Legacy 45-nm

Transition

12-nm

Transition

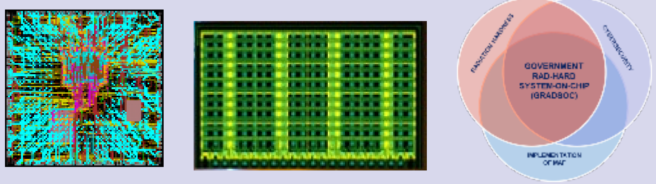
Strategic Neutron SRAM

Transition

Next Generation RHBD Technology Program

- *Sustainment of Legacy 45nm*
- *New sources of technologies enabling onboard processing capability with 100x capability improvement*

Radiation Hardened Standalone Components



SRH SOC

GRADSoC

Transition

GRADSoC Qualification Program

SRH Memory (x3)

Transition

Next Gen High Density RH Memory

RH FPGA Adv. Packaging Solution

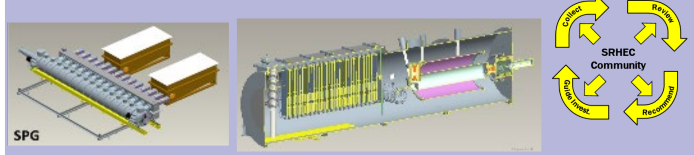
Transition

SRH FPGA

Transition

- *Strategic RH Processor (200x performance)*
- *Memory Products (512 Mb (non-volatile) to 1 Gb (volatile))*
- *SRH Field Programmable Gate Array (FPGA) solutions in support of multiple program needs*

Radiation Hardened Lab Modernization



SPG Facility

Transition – Program Testing

Flash X-ray Facility

Transition – Program Testing

SEE Facility Block Buys & Enhancements

Combined Environments

Library

Newly developed equipment/facilities to provide capacity to the strategic community to address future strategic rad-hard testing demand signal at the national level.

- *Short Pulse Gamma (SPG)*
- *Flash X-Ray*
- *Single Event Effects (SEE)*

LEGEND

Tentative New Starts

Enhanced Capabilities

Sustainment Activity

HW Demonstration ▲ *HW Qualification* ▲ *IOC* ▲

Radiation Hardened Microelectronics Needs

- Next Generation Radiation Hardened Microelectronics with greater performance
- Operational Test
- Larger scale and more capacity

Major Investments to Modernize and Sustain Radiation Hardened Microelectronics

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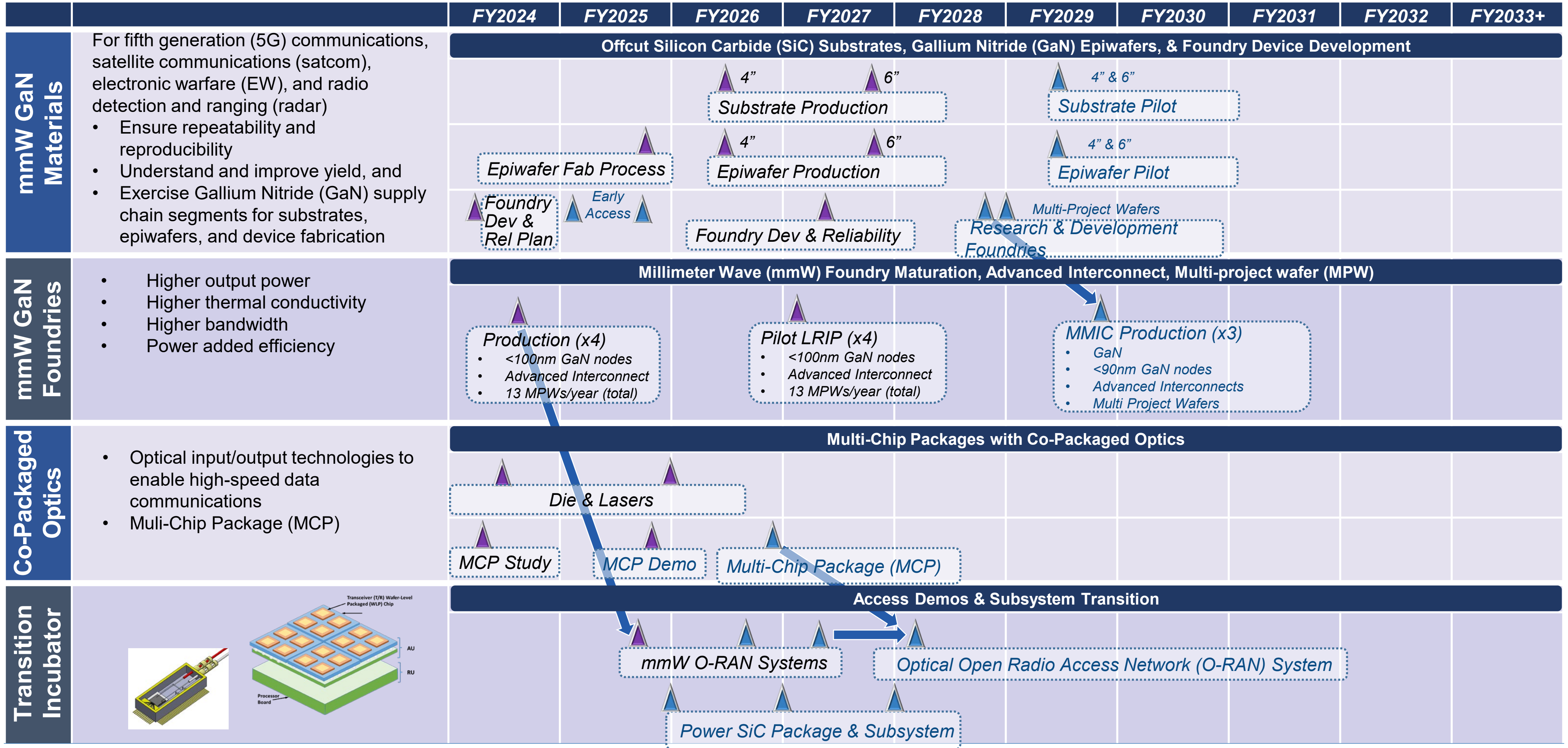
Radio Frequency & Optoelectronics Microelectronics Roadmap



mmW GaN Materials

For fifth generation (5G) communications, satellite communications (satcom), electronic warfare (EW), and radio detection and ranging (radar)

- Ensure repeatability and reproducibility
- Understand and improve yield, and
- Exercise Gallium Nitride (GaN) supply chain segments for substrates, epiwafers, and device fabrication

Offcut Silicon Carbide (SiC) Substrates, Gallium Nitride (GaN) Epiwafers, & Foundry Device Development

4” 6” Substrate Production

4” & 6” Substrate Pilot

Epiwafer Fab Process

4” 6” Epiwafer Production

4” & 6” Epiwafer Pilot

Foundry Dev & Rel Plan

Early Access

Foundry Dev & Reliability

Multi-Project Wafers

Research & Development Foundries

mmW GaN Foundries

- Higher output power
- Higher thermal conductivity
- Higher bandwidth
- Power added efficiency

Millimeter Wave (mmW) Foundry Maturation, Advanced Interconnect, Multi-project wafer (MPW)

Production (x4)
- *<100nm GaN nodes*
- *Advanced Interconnect*
- *13 MPWs/year (total)*

Pilot LRIP (x4)
- *<100nm GaN nodes*
- *Advanced Interconnect*
- *13 MPWs/year (total)*

MMIC Production (x3)
- *GaN*
- *<90nm GaN nodes*
- *Advanced Interconnects*
- *Multi Project Wafers*

Co-Packaged Optics

- Optical input/output technologies to enable high-speed data communications
- Muli-Chip Package (MCP)

Multi-Chip Packages with Co-Packaged Optics

Die & Lasers

MCP Study

MCP Demo

Multi-Chip Package (MCP)

Transition Incubator

Access Demos & Subsystem Transition

mmW O-RAN Systems

Optical Open Radio Access Network (O-RAN) System

Power SiC Package & Subsystem

LEGEND

Enhanced Capabilities

▲ *Key Milestones* ▲ *Options*

Access, mature, & assure Radio Frequency- & Opto-Electronic Microelectronics to enable Spectrum Dominance

Artificial Intelligence/Machine Learning (AI/ML) Hardware Microelectronics Roadmap

	FY2024	FY2025	FY2026	FY2027	FY2028	FY2029	FY2030	FY2031	FY2032	FY2033+

- **Higher energy efficiency,**
- **Higher space efficiency, and**
- **Lower latency microelectronics for faster, more energy-efficient AI**

Broadly adaptable digital energy-efficient edge AI inference systems

~25 prototype devices per year to DoD users; Secure 3U VPX processor cards; software development kit improvements & training; Applications support.

Architecture and design scale-up & optimization for fabrication; Estimated improvements: 5X in performance, 5X in energy efficiency, 10X in single-chip model size; ~100 devices to DoD.

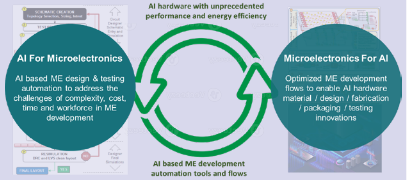
- **>10X improvement in processing efficiency operate reliably within space environments**
- **Support AI/ML workloads**
- **Support real time autonomy for protection, resiliency and assisted decision making**

Neuromorphic compute-in-memory systems for edge AI inference and learning

Develop and demonstrate robust radiation tolerant, low-power and low latency, AI-enabling compute-in-memory systems providing orders of magnitude improved onboard processing capabilities.

Neuromorphic computing systems for integrated AI training and inference at the tactical edge, power AI models and algorithms.

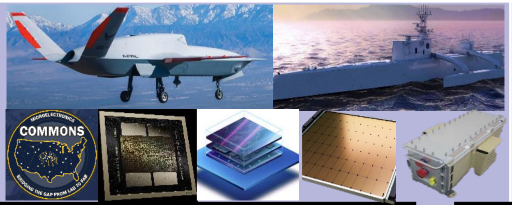
AI-Microelectronics Ecosystem



Development ecosystem: Feedback loop to advance development and AI capabilities

AI based design – Assist to auto-generate and optimize new designs; AI based verification – Automate unit tests, mitigate the increasing need for manpower, enable a broader test coverage; AI based packaging – AI-driven modeling and simulation for predicting performance of design options; Advanced AI hardware – devices & systems for more complex and comprehensive cloud-fog-edge AI compute fabric.

Transition Accelerator



Accelerate the transition of AI hardware to DoD warfighting capabilities.

Public Private Partnerships to inform DoD requirements, AI computing standards, fast prototyping, integration, testing and evaluation; demonstrations and engagements with warfighters.

LEGEND

Enhanced Capabilities

▲ *Key Milestones* ▲ *Options*

AI/ML Hardware Microelectronics Needs

- Size-weight-power-cost efficient edge AI for DoD mission systems
- Cloud-fog-edge AI training and inferencing compute fabric
- AI technologies for Microelectronics development tools, workflows and workforce

DoD's Challenges in Microelectronics

- Commercial industry exploits advances in microelectronics for commercial applications faster than DoD's programs of record in inserting leading-edge microelectronics into weapons systems and platforms; as our adversaries also have access to these advances in microelectronics technologies, **the speed and efficacy of our acquisition process** determines U.S. overmatch capabilities against our adversaries.

- DoD relies on a complex global supply chain for procuring its microelectronics; DoD and the Primes that build systems for the DoD have **limited visibility into the various tiers of the supply chain**; this poses a vulnerability for DoD's microelectronics.

- The CHIPS and Science Act funding to onshore capabilities in microelectronics and the ongoing Trusted and Assured Microelectronics program provide a path forward for **DoD's access to secure microelectronics**; this is a daunting challenge that DoD will address through novel technologies for confidentiality and integrity and a policy framework for assurance of microelectronics.

- It is critical that DoD leverage emerging technologies such as **3D Heterogeneous Integration** as Silicon CMOS scaling has fundamental limits imposed by physics; beyond von-Neumann architectures for edge intelligence applications and beyond Silicon technologies with demonstrated potential for significant improvements in power, performance, area, and cost will ensure DoD's overmatch capabilities.

- DoD's bespoke needs for microelectronics such as strategic radiation hardened microelectronics require a **sharper focus on a workforce in microelectronics** that can support DoD's unique needs and requirements.

- Other countries have increased their investments in technologies such as Gallium Nitride technology to enable next-generation capabilities in Electronics Warfare, Radar, and communication systems; it is imperative that DoD invests sufficiently in these technologies to ensure our adversaries don't have an asymmetric advantage.

- As governments continue to subsidize oversees companies, U.S. Chips and Science Act investments need to assure DoD's microelectronics will have access to an onshore ecosystem that spans design and manufacturing.

Acronyms and Abbreviations

ADK: Assembly Design Kit
AI: Artificial Intelligence
ARPA-E: DOE Advanced Research Projects Agency-Energy
BA: Budget Activity
C4ISR: Command, Control, Communications, Computers, Intelligence, Surveillance, and Reconnaissance
CDR: Critical Design Review
CHIPS: Creating Helpful Incentives to Produce Semiconductors
CMOS: Complementary Metal-Oxide Semiconductor
COTS: Commercial off-the-Shelf
D2TA: Design to Transition Accelerator
DARPA: Defense Advanced Research Project Agency
DIB: Defense Industrial Base
DoD: Department of Defense
DOE: Department of Energy
EDA: Electronic Design Automation
EWD: Education and Workforce Development
FDSOI: Fully Depleted silicon-on-insulator
FPGA: field-programmable gate array
FY: Fiscal Year
GaN: Gallium Nitride
GRADSoC: Government Radiation Hardened System on a Chip
HBCU: Historically Black Colleges and Universities
HI: Heterogeneous Integration
HW: Hardware
IOC: Initial Operational Capability
IoT: Internet of Things
ITAR: International Traffic in Arms Regulations
K-12: Kindergarten through 12th Grade
Lab-to-Fab: Laboratory to Fabrication
LRIP: Low-Rate Initial Production
MCP: Multi-Chip Package
ME: Microelectronics
MEST: Micro-Electronics Security Training (Center)
ML: machine learning
MMIC: monolithic microwave integrated circuit
mmW: Millimeter Wave
MPW: multi-project wafer
MRL: manufacturing readiness level
NIH: National Institutes of Health
NNSA: National Nuclear Security Administration
NSF: National Science Foundation
NSTC: National Semiconductor Technology Center
O-RAN: Open Radio Access Network
PA: Performer Agreements
PD: Principal Director
PD: Professional Development
PDK: Process Design Kit
PDR: Preliminary Design Review
PPAP: Public-Private-Academic Partnership
RAMP: Rapid Assured Microelectronics Prototypes
RAMP-C: Rapid Assured Microelectronics Prototypes-Commercial
RESHAPE: Re-shore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics
RF: Radio Frequency
RFOE: Radio Frequency and Opto-Electronics
RFS: Request for Solutions
RH: Radiation Hardened
RHBD: Radiation Hardened by Design
RINGS: NSF Resilient & Intelligent NextG Systems
R&D: Research and Development
SBIR: Small Business Innovation Research
SC: DOE Office of Science
SDK: software development kit
SEE: single event effects
SHIP: State-of-the-Art Heterogeneous Integrated Packaging
SiC: Silicon Carbide
SOC: system-on-chip
SOI: Silicon on Insulator
SOTP: state-of-the-practice
SPG: short pulse gamma
SRAM: Static Random-Access Memory
SRH: Strategic radiation hardened
STAMP: Stimulating Transition for Advanced Microelectronics Packaging
STEAM PIPE: Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem
STEM: Science, Technology, Engineering, and Mathematics
SW: Software
T&AM: Trusted and Assured Microelectronics
TRL: Technology Readiness Level
USG: United States government
WF: Workforce
YE: Year Ending
YOY: Year over Year